REMARKS

Claims 15-33 are all the claims presently being examined in the application. New claims 27-33 are presented. Claims 15 and 21-26 have been amended to more particularly define the claimed invention.

It is noted that the amendments are made only to more particularly define the invention and not for distinguishing the invention over the prior art, for narrowing the scope of the claims, or for any reason related to a statutory requirement for patentability.

It is further noted that, notwithstanding any claim amendments made herein, Applicant's intent is to encompass equivalents of all claim elements, even if amended herein or later during prosecution.

Claims 15-20 and 22 stand rejected under 35 U.S.C. § 102(e) as allegedly being anticipated by Nakamura et al. (U.S. Patent No. 5,563,422). Claims 23-26 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over by Nakamura et al. (U.S. Patent No. 5,563,422). The Examiner has indicated that claim 21 would be allowable if rewritten in independent form. Accordingly, Applicant has rewritten claim 21 as suggested by the Examiner.

These rejections are respectfully traversed in view of the following discussion.

I. THE CLAIMED INVENTION

Applicant's invention, as disclosed and claimed, is directed to a method for manufacturing a light-emitting semiconductor device of Group III nitride compound semiconductor with p-type conduction.

In one aspect, as recited in amended claim 15, the method includes providing a surface layer, forming a multi-layered electrode layer comprising a first electrode layer

formed on the surface layer and a second electrode layer formed on the first electrode layer, the first electrode layer comprising a material having ionization potential lower than that of the second electrode layer and the second electrode layer comprising a material having an ohmic characteristic to the semiconductor better than that of the first electrode layer, forming an electrode pad covering a portion of the second electrode layer and leaving another portion of the second electrode layer uncovered; moving an element of the first electrode layer to near a surface of the multi-layered electrode layer and penetrating an element of the second layer into the surface layer to be metallized with Group III nitride compound semiconductor as a reaction of the moving an element of the first electrode layer, by a heat treatment; and making a distribution so that the portion of the material of the second electrode layer which is uncovered by the electrode pad is distributed more deeply into the surface layer than that of the first electrode layer and provides a contact resistance between the electrode layer and the surface layer lower than the portion covered with the electrode pad.

In another aspect of the claimed invention, as recited in amended claim 27, the method includes, inter alia, "selecting an element of a first electrode layer having an ionization potential that is lower that that of an element of a second electrode layer and selecting said element of said second electrode layer having better ohmic contact to said Group III nitride compound semiconductor than said element of said first electrode layer."

The claimed invention provides a contact resistance between the electrode layer and the surface layer lower than the portion covered with the electrode pad by making a distribution by heat treatment such that the portion of the material of the second electrode layer which is uncovered by the electrode pad is distributed more deeply into the surface layer than that of the first electrode layer. Accordingly, the portion of the electrode layer under the electrode pad has poor ohmic characteristics (e.g. high contact resistance), thereby

causing the flow of electric current around that portion. This feature enables the electric current to flow to effective portions of the device that emit light to the outside. As a result, the luminous efficiency is improved. (Application at page 5, lines 1-16)

Additionally, by moving an element of the first electrode layer to near a surface of the multi-layered electrode layer and penetrating an element of the second layer into the surface layer to be metallized with Group III nitride compound semiconductor, the adhesion between the electrode and semiconductor is greatly improved. (Application at page 7, lines 7-16)

II. THE PRIOR ART REJECTIONS

A. The Nakamura et al. Reference

The Examiner alleges that the claimed invention is anticipated by the Nakamura et al. reference and/or rendered obvious by Nakamura et al. However, Applicant respectfully submits that the reference does not teach or suggest each and every element of the claimed invention.

Nakamura et al. appears to disclose a gallium nitride-based III-V Group compound semiconductor device having a gallium nitride-based III-V Group compound semiconductor layer provided over a substrate, and an ohmic electrode provided in contact with the semiconductor layer wherein the ohmic electrode is formed of an annealed metallic material. (Nakamura et al. at Abstract)

However, regarding claim 15, Nakamura et al. does not disclose or suggest that an element (e.g. atoms) of the first electrode layer is moved to near (e.g. shifted around) the surface of the multi-layered electrode layer, that an element (e.g. atoms) of the second electrode layer is penetrated into the surface layer which is made of a Group III nitride compound semiconductor as its counteraction, and that an element (e.g. atoms) of the second

electrode layer is metallized (e.g. alloyed) with an element (e.g. atoms) of the Group III nitride compound semiconductor, as in the claimed invention.

Moreover, Nakamura fails to disclose or suggest that a portion of (e.g. atoms) the second electrode layer distribute and penetrate in the Group III nitride compound semiconductor deeper than that (e.g. atoms) of the first electrode layer.

Further, such an inverted distribution occurs at the portion of the second electrode layer where no electrode pad is formed. At the portion immediately under the electrode pad, atoms of the first electrode layer and atoms of the second electrode layer are distributed in sequence. Such features are not disclosed or suggested in Nakamura et al.

Accordingly, the contact resistance of the portion covered with the electrode pad is higher than the portions not covered by the electrode pad. Hence, electric current does not flow under the electrode pad toward the Group III nitride compound semiconductor in the present invention.

Additionally, with regards to new claim 27, Nakamura et al. does not disclose or suggest forming the first electrode layer by using a material (e.g. atoms) whose ionization potential is lower than that of the material (e.g. atoms) which constitutes the second electrode layer, as recited in the claimed invention.

Further, Nakamura fails to teach or suggest that the second electrode layer is formed using a material (e.g. atoms) whose ohmic contact toward the Group III nitride compound semiconductor is smaller or better than that of the material (e.g. atoms) of the first electrode layer, as in Applicant's claimed invention.

Additionally, in Nakamura's invention, the electrode layer 15 comprises 0.1μm in thickness of Ni (nickel) and 0.1μm in thickness of Au (gold) (Nakamura at column 7, embodiment 2). In a non-limiting exemplary aspect of the present invention, the first

electrode layer 81 is Ni (nickel) having a thickness of 25Å, and the second electrode 82 is Au (gold) having a thickness of 60Å. A thickness of the first electrode layer 81 is about 1/40 of that of Nakamura's Ni layer, and a thickness of the second electrode layer 82 is about 1/20 of that of Nakamura's Au layer. Accordingly, because the thicknesses of the layers are completely different from those in Nakamura's invention, no distribution dislocation occurs in Nakamura's invention.

When the second electrode layer is formed thicker, for example, about 1000Å, atoms in the first electrode layer cannot easily be shifted to the surface of the layer in a short time even if a lower ionization potential of the atoms is used in the first electrode layer. In short, because atoms of the first electrode layer are not influenced by the atmosphere, those atoms having a lower ionization potential do not shift to the atmosphere side.

Accordingly, the atoms which form the first electrode layer are shifted to its surface, and as a counteraction the atoms of the second electrode layer are penetrated more deeply (e.g. more deeply than the atoms of the first electrode layer) into the Group III nitride compound semiconductor. Such a feature is clearly not suggested by Nakamura's invention which discloses a thicker electrode layer.

Therefore, Applicant submits that the Nakamura et al reference does not teach or suggest each and every element of the claimed invention. Therefore, the Examiner is respectfully requested to withdraw the rejections.

III. FORMAL MATTERS AND CONCLUSION

Applicant notes that the Examiner has failed to acknowledge the foreign priority of the present application. The present application is a divisional of Application No. 08/866,129 (now issued as U.S. Patent No. 6,734,468) which based its priority claim on Japanese

Application Number JP160885/1996 filed on May 31, 1996. The Examiner is respectfully requested to acknowledge the claim for foreign priority in this application.

In view of the foregoing, Applicant submits that claims 15-33, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

Date: 1/31/05

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